Electronic Version
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Claims

[c1] 1. A method of forming a contact opening, comprising the steps of:
providing a substrate having a plurality of conductive structures formed thereon;
performing an ion implantation;
performing a thermal processing operation for forming a liner layer on the sidewalls of the conductive structures and the exposed substrate, wherein the liner layer on the sidewalls of the conductive structures has a thickness smaller than the liner layer on the substrate surface;
forming an insulation layer over the substrate that also covers the conductive structures; and
patterning the insulation layer so that a contact opening is formed between two neighboring conductive structures.

[c2] 2. The method of claim 1, wherein the step of performing an ion implantation further comprises:
performing an ion implantation with the ion beam tilted at an angle relative to the implanting surface such that ions are implanted into the sidewalls of the conductive structures and the cap layers, wherein the implanted

ions has a capability of inhibiting the growth of the oxide film during the thermal processing operation.

[c3] 3. The method of claim 2, wherein the ions implanted into the sidewalls of the conductive structures comprises nitrogen ions.

[c4] 4. The method of claim 1, wherein the step of performing an ion implantation further comprises:
performing a vertical ion implantation for implanting ions into the substrate between neighboring conductive structures, wherein the ions has a capability of enhancing the growth of the oxide film during the thermal processing operation.

[c5] 5. The method of claim 4, wherein the ions implanted into the substrate between neighboring conductive structures comprises oxygen ions or argon ions.

[c6] 6. The method of claim 1, wherein the step of forming the conductive structures comprises:
forming a gate dielectric layer, a polysilicon layer, a metal silicide layer and a silicon nitride layer over the substrate;
patterning the silicon nitride layer; and
patterning the metal silicide layer and the polysilicon layer to form a plurality of gate structures such that each

gate structure has a cap layer.

[c7] 7. The method of claim 1, wherein before the step of performing the ion implantation, further comprises a step of performing a metal silicide etching operation to remove a portion of the sidewall metal silicide layer.

[c8] 8. The method of claim 1, wherein after the step of performing the ion implantation, further comprises a step of performing a metal silicide etching operation to remove a portion of the sidewall metal silicide layer.

[c9] 9. The method of claim 1, wherein after the step of forming the liner layer on the sidewall of the conductive structures and the surface of the substrate, further comprises:
forming a spacer on the sidewall of the conductive structures;
forming an insulation layer over the substrate to cover the conductive structures; and
patterning the insulation layer to form a self-aligned contact opening between a pair of neighboring conductive structures.

[c10] 10. The method of claim 1, wherein the thermal processing operation comprises a step of performing a rapid thermal annealing operation followed by a rapid thermal

oxidation.

[c11] 11. A method of manufacturing a semiconductor device, comprising the steps of:
providing a substrate having a plurality of gate structures formed thereon, wherein each gate structure has a cap layer thereon;
performing an ion implantation; and
performing a thermal processing operation to form a liner layer on the sidewalls of the conductive structures and the exposed substrate, wherein the liner layer on the sidewalls of the conductive structures has a thickness smaller than the liner layer on the substrate surface.

[c12] 12. The method of claim 11, wherein the step of performing an ion implantation furthermore comprises:
performing a tilt ion implantation for implanting ions into the sidewalls of the gate structures and the cap layers, wherein the implanted ions has a capability of inhibiting the growth of the oxide film during the thermal processing operation.

[c13] 13. The method of claim 11, wherein the ions implanted into the sidewalls of the gate structures comprises nitrogen ions.

[c14] 14. The method of claim 11, wherein the step of per-

forming an ion implantation further comprises:
performing a vertical ion implantation for implanting ions into the substrate between neighboring gate structures, wherein the ions has a capability to enhance the growth of the oxide film during the thermal processing operation.

[c15] 15. The method of claim 14, wherein the ions implanted into the substrate between neighboring gate structures comprises oxygen ions or argon ions.

[c16] 16. The method of claim 11, wherein the step of forming the gate structures comprises:
forming a gate dielectric layer, a polysilicon layer, a metal silicide layer and a silicon nitride layer over the substrate;
patterning the silicon nitride layer; and
patterning the metal silicide layer and the polysilicon layer.

[c17] 17. The method of claim 11, wherein before the step of performing the ion implantation, further comprises a step of performing a metal silicide etching operation to remove a portion of the sidewall metal silicide layer.

[c18] 18. The method of claim 11, wherein after the step of performing the ion implantation, further comprises a

step of performing a metal silicide etching operation to remove a portion of the sidewall metal silicide layer.

[c19] 19. The method of claim 11, wherein the thermal processing operation comprises a step of performing a rapid thermal annealing operation followed by a rapid thermal oxidation.